

**REMARKS**

Claims 1-24 are all the claims pending in the application.

Based on the Response filed April 12, 2004, the Examiner repeated the previous claim rejection. The status of the claims is the following.

Claims 7-10, 17-20, 23 and 24 are allowed.

Claims 1 and 11 are rejected under 35 U.S.C. § 102(e) as being anticipated by previously-cited Roylance et al. (US 6,390,579; hereafter "Roylance").

Claims 2-6, 12-16, 21 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In the Response filed April 12, Applicant argued that Roylance does not disclose a pulse width modulating signal output device which makes a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the processing clock signal generated by an operation device, and makes the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the processing clock signal generated by the operation device, as recited in claim 1. In the "Response to Arguments" on pages 3-4 of the Office Action, the Examiner points to FIG. 1 of Roylance and argues that FIG. 1 shows a pulse width modulator 10 including a Pclock which generates a first clock 20, an operation device 25, 36, which operates the first clock signal and generates at least one processing clock going into 18 a PWM output device 24 (composed of 12, 18, 38, 40, and 42), which makes a pulse of a PWM signal rise synchronously with a remaining one of the first clock signal Pclock and the

**RESPONSE UNDER 37 C.F.R. § 1.116**  
**U. S. Application No. 09/556,821**

processing clock out of 25 into 18 generated by the operation device 25, 36 (col. 4, lines 9-15, 22-62). Applicant disagrees with the Examiner's assessment and has the following comments.

Applicant submits that neither FIG. 1, nor the specification, of Roylance discloses or suggests a pulse width modulating signal output device which makes a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the processing clock signal generated by an operation device, and makes the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the processing clock signal generated by the operation device. Although the Examiner has asserted that Roylance discloses all of these features of the claim, the Examiner has not supported his assertions. The alleged disclosures referred to by the Examiner merely show that FIG. 1 of Roylance illustrates a clock signal Pclock input into an adjustable delay 25 of a pulse width modulator 10. The signal output from adjustable delay 25 is input into flip-flops 18 and 36. After a series of exclusive-OR gates, a PWMout signal is output from the pulse width modulator 10. Furthermore, the only figure of Roylance that illustrates timing relationships for Pclock (FIG. 3) illustrates a relationship in which Pclock and PWMout do not rise or fall synchronously in any way. Applicant submits that Roylance simply fails to teach or suggest this claimed feature of claim 1, and thus, claim 1 is not anticipated by Roylance.

Further, claim 11 is not anticipated for reasons analogous to those presented above for claim 1.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

**RESPONSE UNDER 37 C.F.R. § 1.116**  
**U. S. Application No. 09/556,821**

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

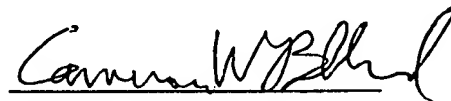
Respectfully submitted,

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**23373**

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